What is claimed is:

1. Apparatus, comprising:

an analog sampling array, for acquiring from a signal under test (SUT) a plurality of temporally offset analog samples during each of a sequence of sample periods;

a plurality of sample processors, for identifying logic level transitions between respective current and previous samples and for determining a time of occurrence of said logic level transitions.

2. The apparatus of claim 1, further comprising:

a time stamp processor, for imparting a time stamp to sample data indicative of respective sample times.

3. The apparatus of claim 1, wherein said samples are acquired and logic level transitions identified in real time.

4. The apparatus of claim 1, wherein sample intervals are defined as respective temporal portions of a period of a logic clock (LCLK).

5. The apparatus of claim 1, wherein:

for each sample period, each sample processor receives a respective current sample (V_C) and a respective previous sample (V_P) and responsively produces sample data comprising indicia of the logic level of the current sample (L), any identified logic level transition between the current and previous samples (E) and an estimated time of occurrence of said identified logic level transition (TPE).

6. The apparatus of claim 5, further comprising:

reduction logic, for reducing the amount of data provided to said time stamp processor by discarding sample data not associated with an identified logic level transition.

7. The apparatus of claim 6, further wherein:

sample data produced by each sample processors is associated with a respective slice identifier.

8. The apparatus of claim 1, further comprising:

sample point and violation detection logic (SPVDL) for determining if sample data provided by said sample processors conforms to at least one rule.

9. The apparatus of claim 1, wherein a system comprising a plurality of instances of said apparatus are used to process respective signals under test including at least one clock signal and at least one data signal; and wherein:

a logic event recognizer receives data from said system and responsively produces an indication of the presence of a logic event.

10. A method, comprising:

acquiring a plurality of temporally offset analog samples of a signal under test (SUT) during each of a sequence of sample periods;

determining a logic level for each of said analog samples using a threshold signal level; and

generating an edge bin data structure for at least those analog samples having a logic level different from respective immediately preceding analog samples;

each edge bin data structure including identification of a sample associated with said logic level transition and an estimation of the relative threshold level crossing time of the SUT between successive samples.

11. The method of claim 10, wherein an edge bin is generated for each of said temporally offset analog samples of said SUT during each of said sequence of sample periods, said method further comprising:

discarding those edge bins associated with analog samples having the same logic level as respective immediately preceding analog samples.

12. The method of claim 10, wherein:

in the case of a SUT comprising a data signal, said edge bin data structure further includes a logic level indicator.

13. The method of claim 10, wherein:

said edge bin data structure comprises a time stamp indicative of the time of a respective threshold level transition of said SUT within said sample period;

said edge bin data structures adapted to enable thereby mathematical adjustment of temporal data.

14. The method of claim 10, wherein said method is used to process each of a plurality of signals under test including a clock signal and at least one data signal to produce corresponding lists of edge bins, said method further comprising:

processing each data signal edge bin list with said clock signal edge bin list to identify, for each clock signal edge, a corresponding logic value of said data signal.

15. The method of claim 14, further comprising:

processing each data signal edge bin list with said clock signal edge bin list to identify a timing violation.

16. The method of claim 10, wherein:

said a timing violation comprising at least one of a setup-and-hold violation and a glitch.

17. The method of claim 14, further comprising:

examining the logic values of at least a portion of said data signals under test to determine whether a logic event has occurred.

18. The method of claim 17, wherein:

said logic event comprises the occurrence of at least one of a logical word and a change in a logical word.

19. The method of claim 14, further comprising:

in response to a temporal offset command, modifying said clock signal edge bin list to impart thereby a temporal clock edge shift.

20. The method of claim 19, wherein:

said clock signal edge bin list is modified by adjusting each edge bin according to an edge bin value representing an amount of said temporal shift

21. The method of claim 14, further comprising:

associating each clock signal edge bin with a time stamp derived from a counter incremented according to a logic clock.